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## Architecture Paradigms and Programming Languages for Efficient programming of multiple COREs

Specific Targeted Research Project (STReP)

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### Publication of the Microgrid emulation platform

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Workpackage WP5

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**Purpose:** The purpose of this deliverable is to document the publication of the Microgrid emulation platform by the University of Amsterdam.

**Results:** The main results of this deliverable are the Microgrid emulation platform.

**Conclusion:** The conclusion this deliverable is the delivery of the Microgrid emulation platform.

**Approved by the project coordinator:** Yes      **Date of delivery to the EC:** 2008-12-31

## Document history

When	Who	Comments
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The purpose of this deliverable is to document the publication of the Microgrid emulation platform.

## 1 The Microgrid Emulation Platform

The Microgrid emulation platform has been developed at the University of Amsterdam to emulate a ring of microthreaded processors as an ISA-based implementation of the Sane Virtual Processor (SVP) model.

### 1.1 Features

The features of the emulation platform are:

- Cycle-accurate simulation of a grid of microthreaded Alpha processors.
- Support for loading ELF or flat binaries.
- Able to step through the execution of the system cycle-by-cycle.
- Inspect the state of the system during execution, including pipeline, registers, memory.
- Performance report of an executed program.
- Packaged with GNU binutils 2.18 for support the Microthread Alpha binary formats.
- Extensive configurability such as: number of number of processors on the grid, latency of FPU operations, number of threads and families per processor, cache size and layout, memory implementation.
- Reporting of deadlock situations.
- Reporting of invalid instructions in the executed program.
- Reporting of undefined behavior such as reading from empty registers.
- Modular and extensible design and implementation allows for easy modifications to pursue different research directions.

### 1.2 SVP conformance

The emulation platform conforms to the SVP model on the following points:

- Family creation on local and default place, family termination and synchronisation
- Shared and global argument passing.
- Sharing across threads in a family.
- Asynchronous memory consistency scheme according to SVP specification.
- Automatically computes thread index and makes it available to the thread.

## 2 Publication details

The emulation platform described in the previous section has been published both internally and externally to the project. Internally, partners can obtain the source code and assistance from the University of Amsterdam partner. Externally, a build of the emulation platform for Windows along with some documentation and several example assembly files has been published on-line at [http://www.apple-core.info/?page\\_id=7](http://www.apple-core.info/?page_id=7).